DRAMs in Chip-Size Packages

Satisfying Diverse Application Needs

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San Jose January 23-24, 2001 • Taipei February 14-15, 2001

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Infineon at a Glance

Infineon Technologies

- Top 10 semiconductor company
- One of the fastest growing semiconductor companies
- 27,000 employees
- World class manufacturing sites on three continents

Memory Products

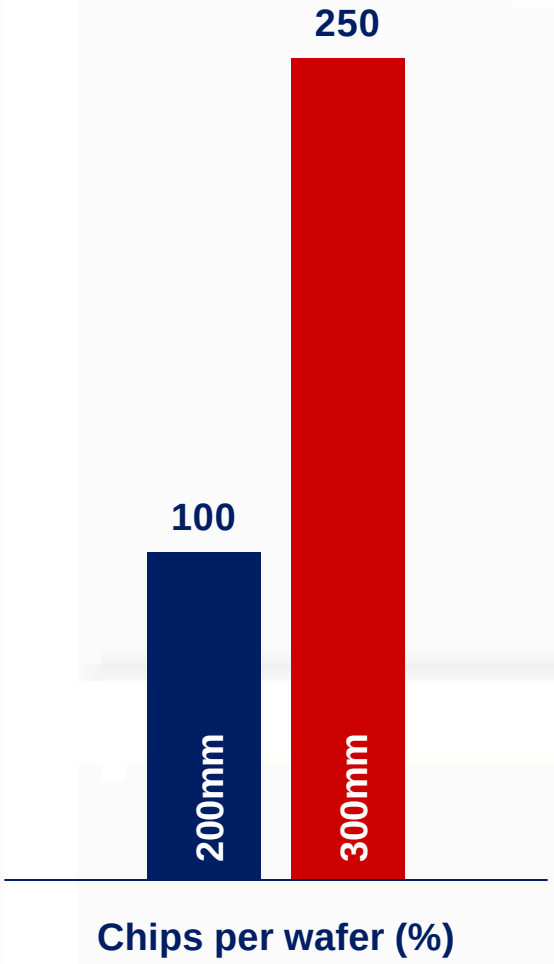
- World-wide # 5 DRAM manufacturer (Dataquest)
- World-wide # 1 in 256M manufacturing volume
- Leader in embedded DRAM and 300mm technology
- Four 8-inch fabs running 0.17µm process technology
- First company worldwide to ship fully qualified 64M SDRAM from 300mm pilot line in Dresden

World Leader in 300mm Production

New 300mm Module in Dresden

Total Investment	**$ 1.1bn**
Construction Date	**June 2000**
Capacity	**up to 6,000 WSPW**
Employees	**1,100**
Technology	**Ramp up 256M in 0.14µm**
Volume Production	**512M / 1G in 0.11 / 0.09µm**

Cost reduction per chip ? 30%

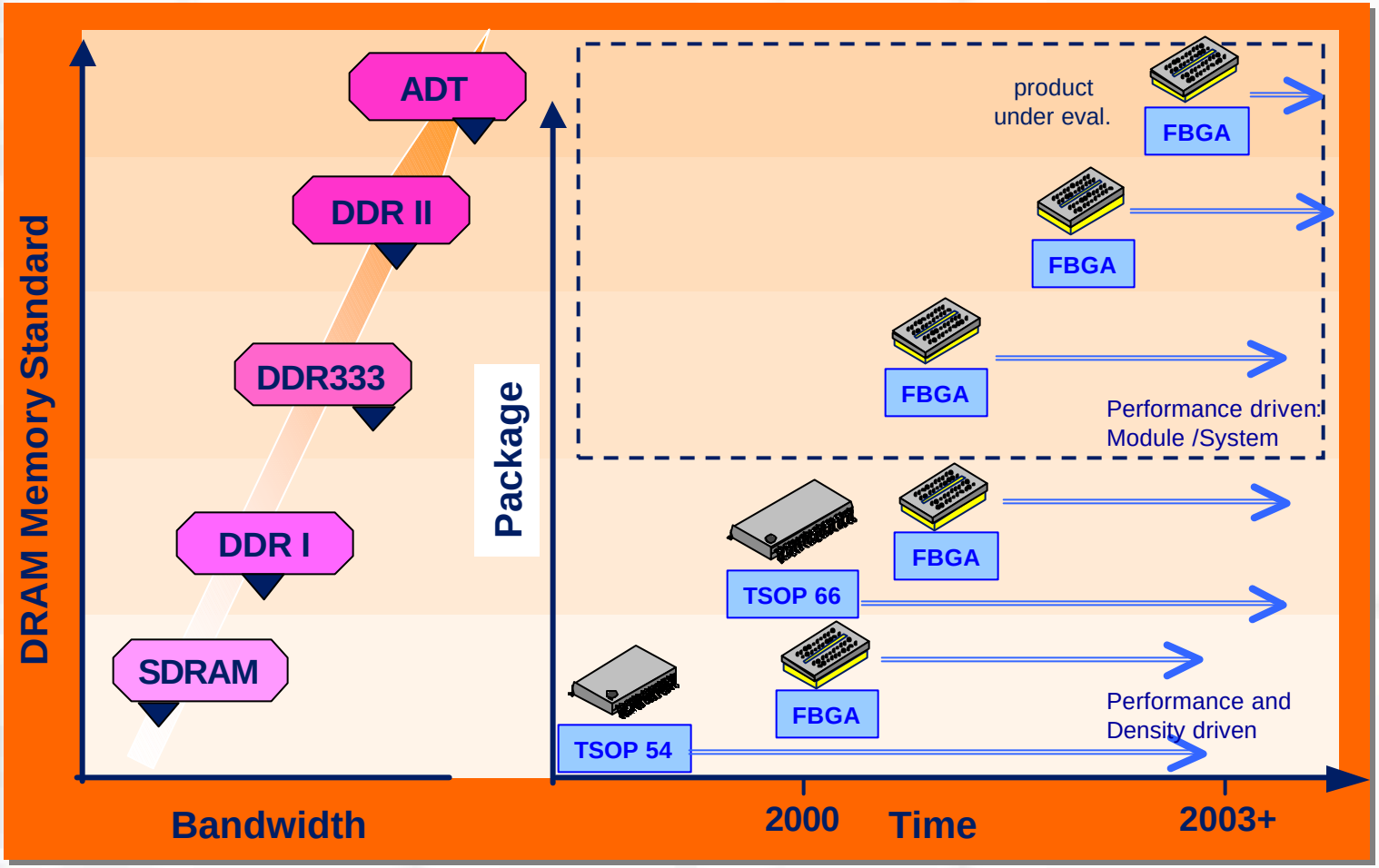


Chips per wafer (%)

- Infineon at a Glance
- **Infineon's Chip Size Package: BOC**
- CSP enables High-Density Modules
- Low-Power Mobile-RAM
- DDR Products using CSP
- CSP enables speedy 128M SGRAM

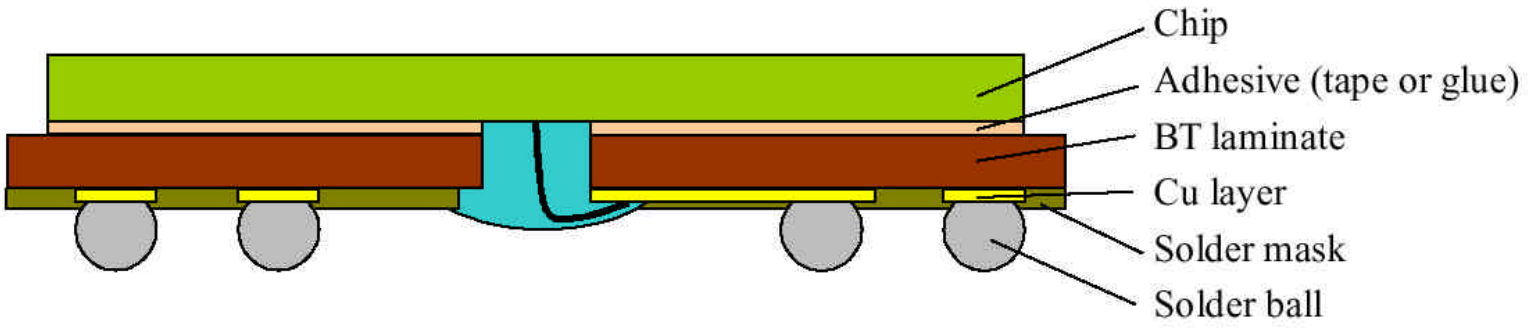
Memory Packages Overview

Packages for Standard DRAMs by Architecture



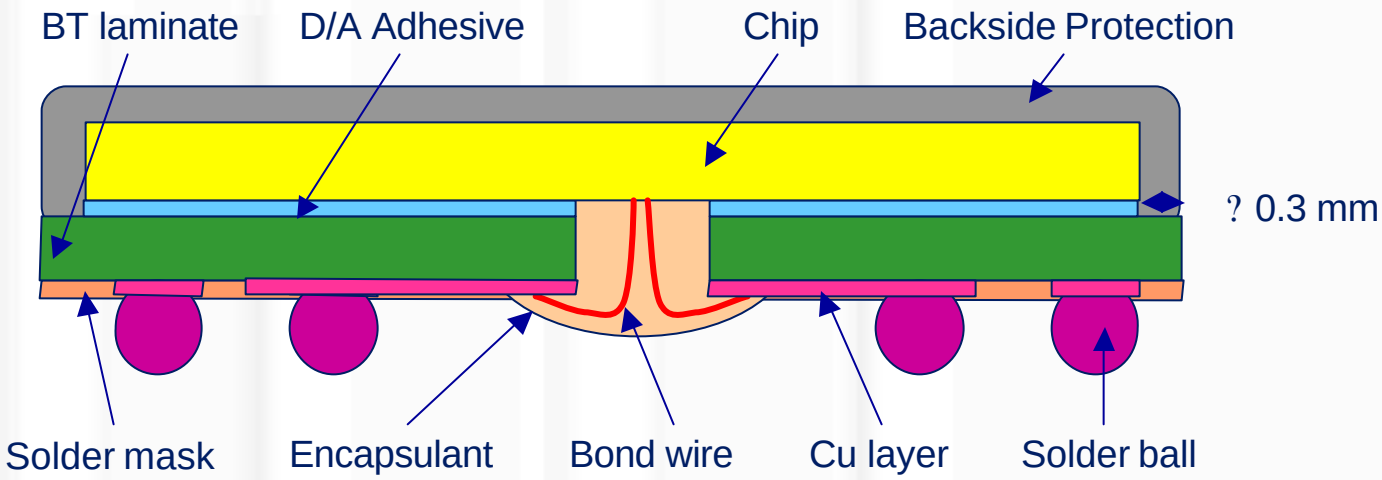
- Driven by operating speed and packing density, FBGA package technology will evolve as new DRAM standard package

Infineon's Chip-Size-Package
Board-on-Chip



- Board-On-Chip (BOC) technology uses Wire-bonding
- Advantages of wire-bonding compared to lead-bonding:
  - Improved Reliability
  - Reduced Cost

FBGA-BOC Features



- For Applications requiring more rugged packages, the back side of the chip may be protected
- Key Features (comparisons to TSOP package):
  - Smaller, less weight
  - Shorter electrical and thermal paths
  - Improved electrical and thermal performance (R, L, C, ? ja)

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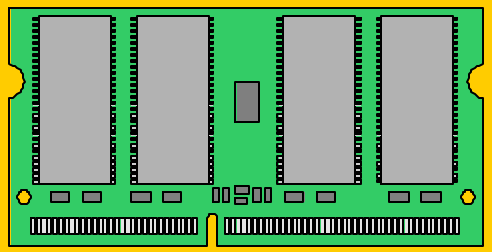
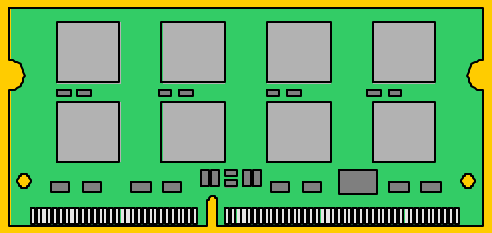
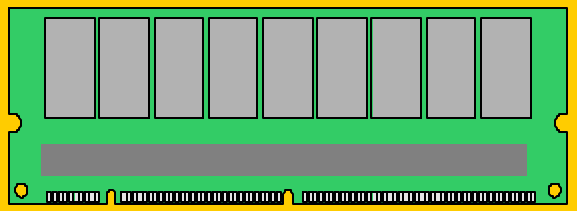
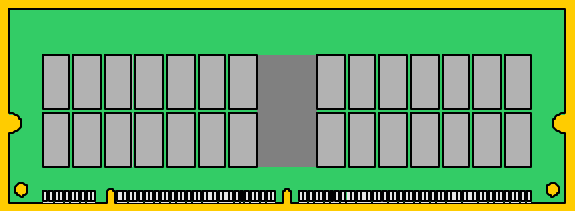
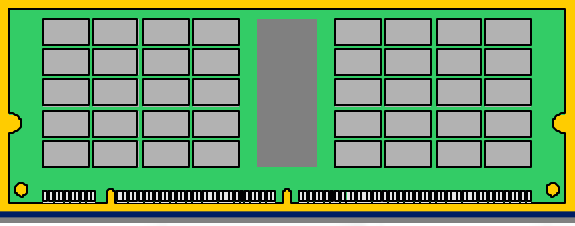
- Low-Power Mobile-RAM
- DDR Products using CSP
- CSP enables speedy 128M SGRAM

SO-DIMM Population Variants

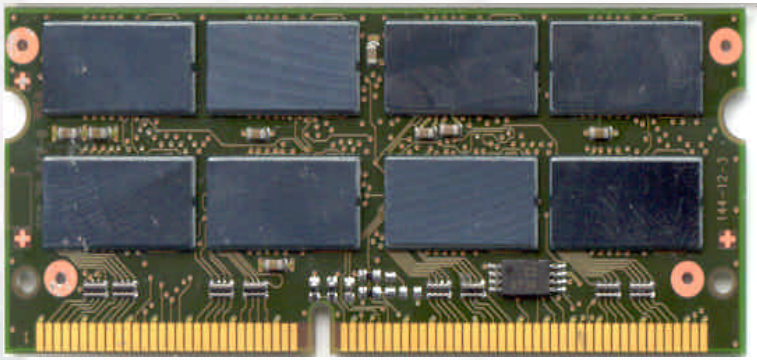
SDRAM SO-DIMM 67.6 mm x H x 3.8 mm	Module Density Considerations for 128M DRAM	
	Package type, Nr. of devices / side	**Module Density**
	**TSOP 400mil** 11.76 mm x 22.22 mm 4 components SO-DIMM H=31.75 mm	128 MB **x1** “Standard Density“
	**FBGA** 7 mm x 9 mm 8 components SO-DIMM	256 MB **x2** “Doubled Density“

Registered DIMM Population Variants

SDRAM Registered DIMM 133.35 mm x 43.18 mm x T	Considered die size: 5.8 mm x 11 mm	
	Package type, **Nr. of devices / side**	**Module** **Density**
	**TSOP** 400mil 11.76 mm x 22.22 mm 9 components 18 comp. w/ stacking	Standard density **Stacked**: doubled density
	**FBGA** 6.5 mm x 12 mm 18 components	**FBGA-BOC** ? doubled density w/o stacking
	**True CSP** (die-sized) 5.8 mm x 11 mm 36 components	**True CSP** ? **potential for additional doubling of memory density**

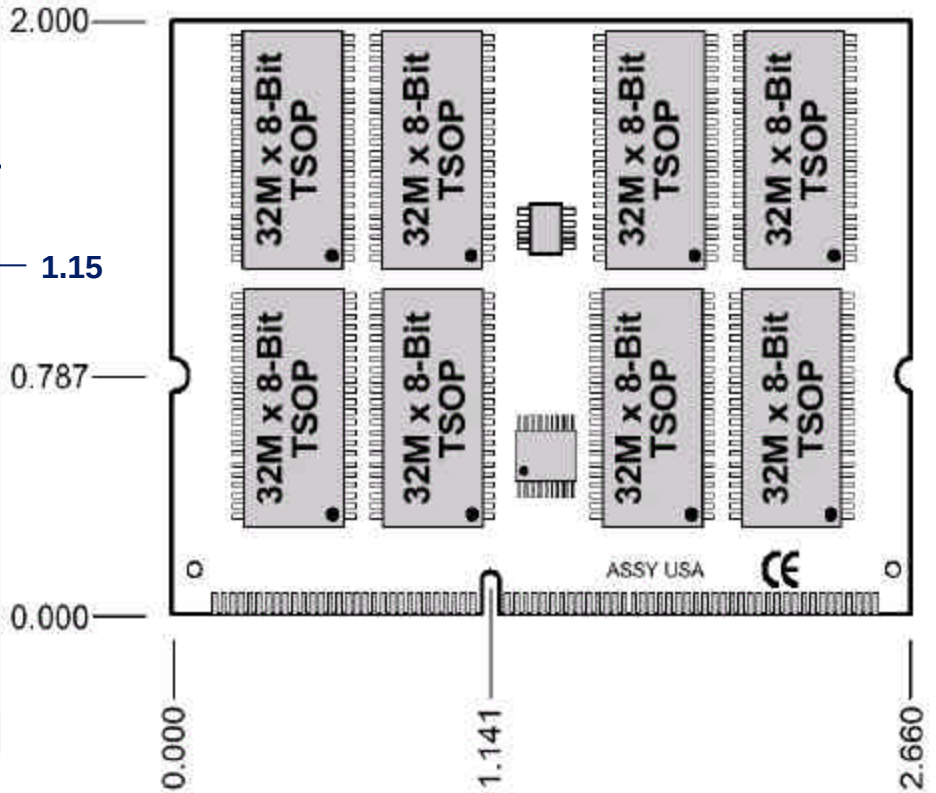
FBGA vs. TSOP: 512MB SODIMM

512MB SODIMM
based on 256M SDRAM @ 0.17µ



Future Infineon Product

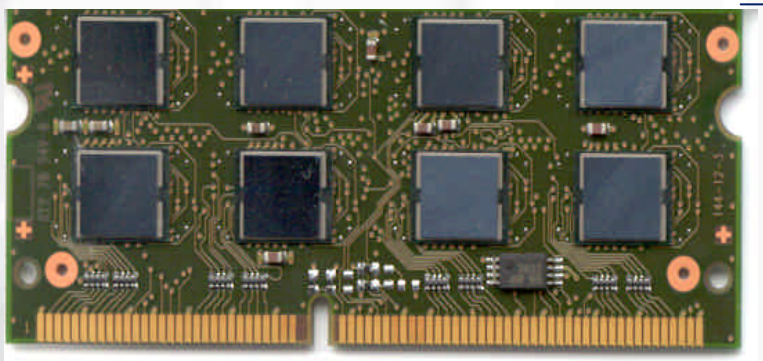
512MB SODIMM
(non-Infineon)



256MB SODIMM Chip Size Comparison

- Small die size allows to build smaller form-factor modules

256MB SODIMM
based on 128M SDRAM @ 0.17µ

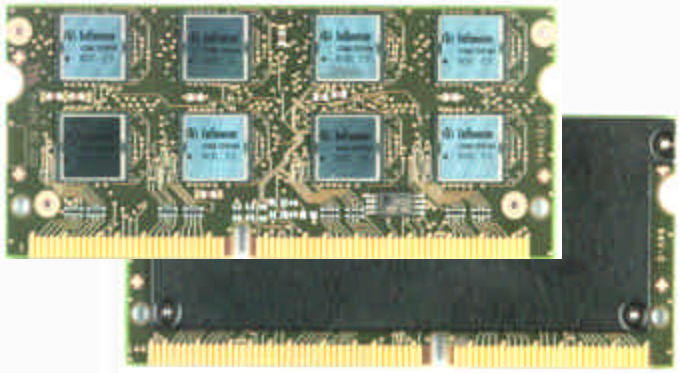


Future Infineon Product

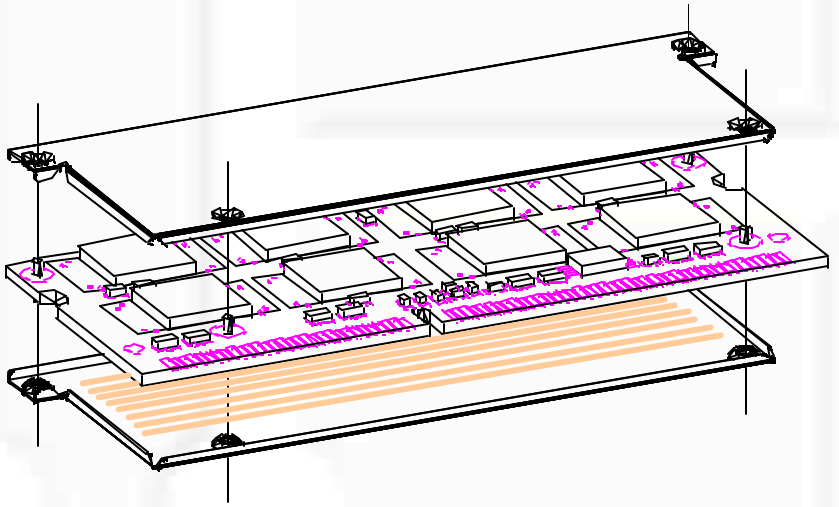
256MB SODIMM
(non-Infineon)

1.25
1.15

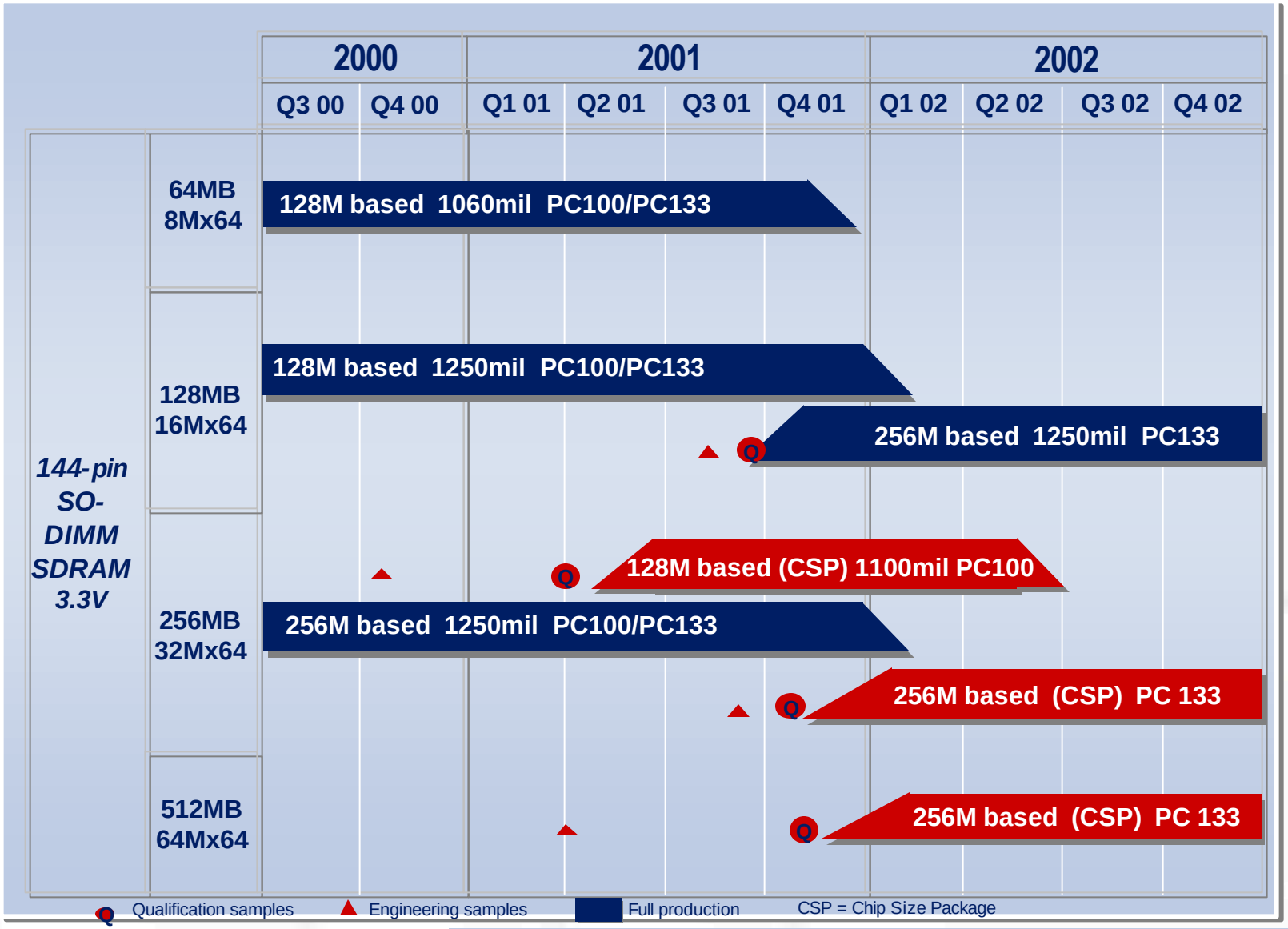
FBGA-BOC for High-Density SO-DIMM



- Optional aluminum plates add two important benefits
  - mechanical protection for memory chips
  - act as heat spreader if required



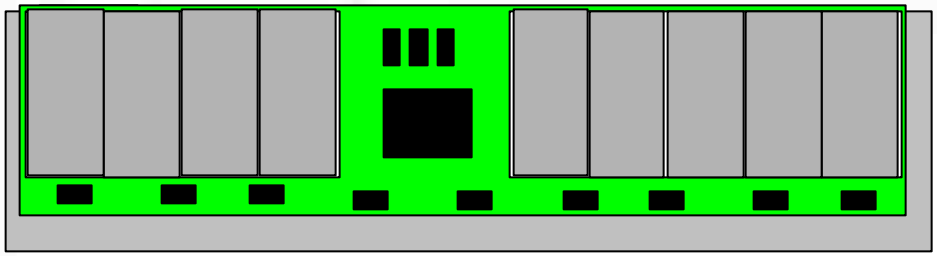
Infineon Product Roadmap: SO-DIMMs



1U-DIMM (Reduced Height 1.2“)

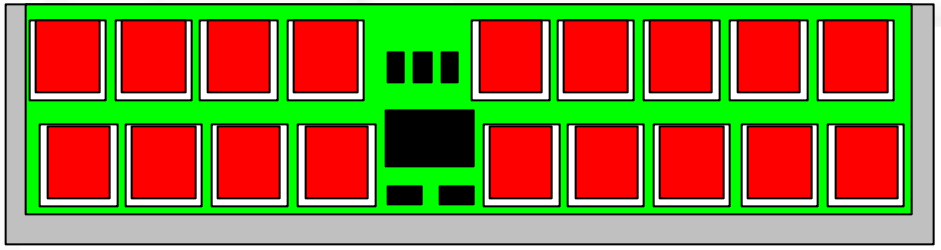
TSOP-based

- Standard for SDR SDRAM
- max 512MB non-stacked
- max 1GB stacked
  (for 256M components)



BOC-based

- Planned for DDR SDRAM
- max 1 GB non-stacked
  (for 256M components)



- Infineon at a Glance
- Infineon’s Chip Size Package: BOC
- CSP enables High-Density Modules
- **Low-Power Mobile-RAM**
- DDR Products using CSP
- CSP enables speedy 128M SGRAM

Mobile-RAM: Key Features

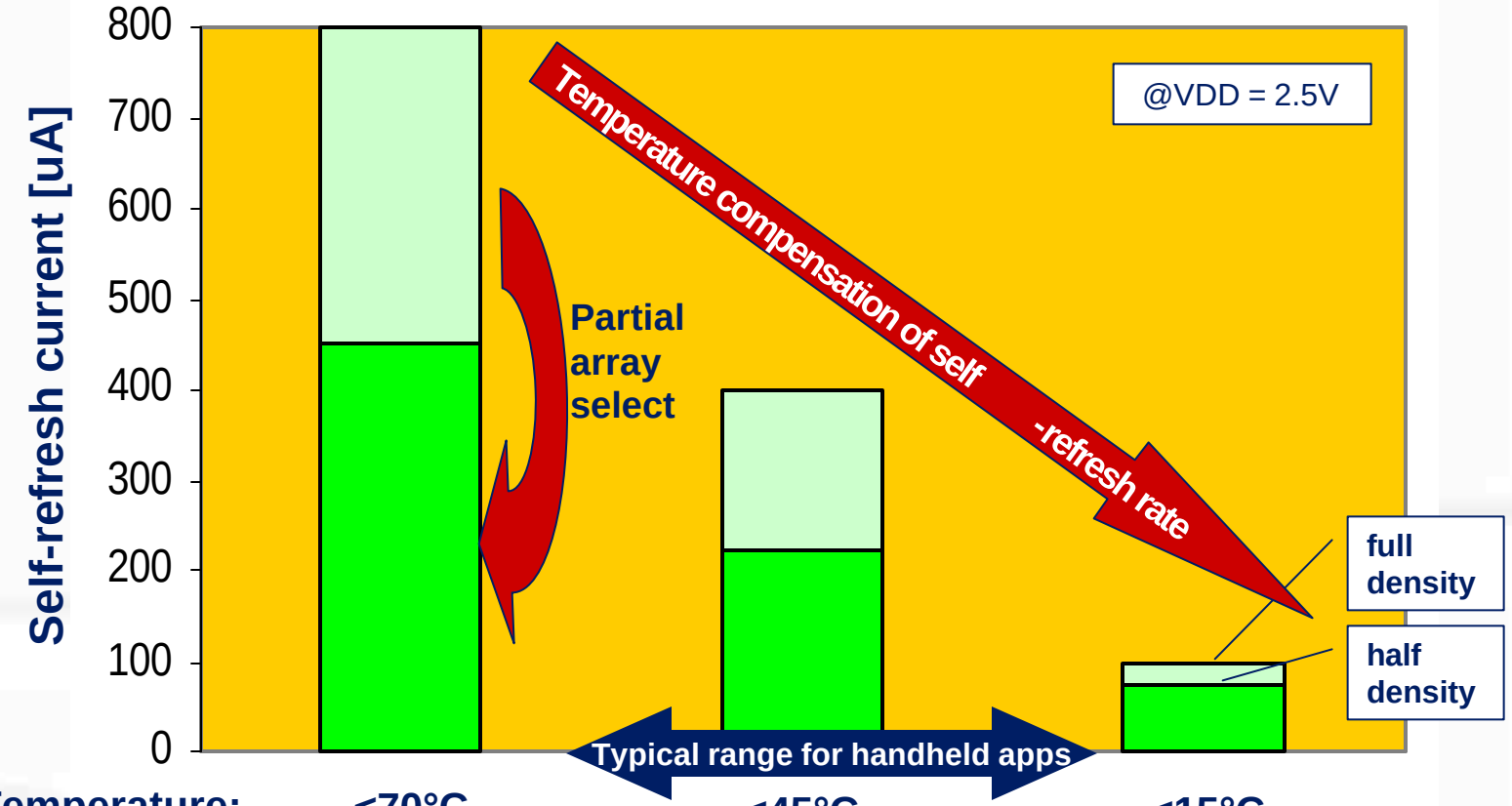
- First Product: 128M density
  - 0.17?m technology
  - SDRAM 8Mx16 (includes x4, x8 options)
  - Supply Voltage VDD = 2.5V
  - I/O Voltage VDDQ = 1.8V (2.5V tolerant)
  - Standard SDRAM interface
  - Reduced self-refresh current
  - Special Mobile-RAM features for low power management
  - 54-ball chip-size-package/BGA
- 256M follow-on product planned
- JEDEC standardization imminent

Mobile-RAM Low Power Features

- Operating current reduced by design
- Reduction of refresh current
  - Partial array select
    - Idea: Select only 64Mbit out of 128Mbit device
      ? up to 45% power reduction for 4 vs 2 bank enabled
  - Temperature compensated Self-Refresh
    - Idea: reduced refresh rate at lower temperatures using external sensor (available in application)
      ? up to 85% power reduction
    - Note: In standard DRAMs the refresh-rate is optimized for cell leakage at high temperatures i.e. worst conditions
- Offers 25% to 85% reduction of current consumption

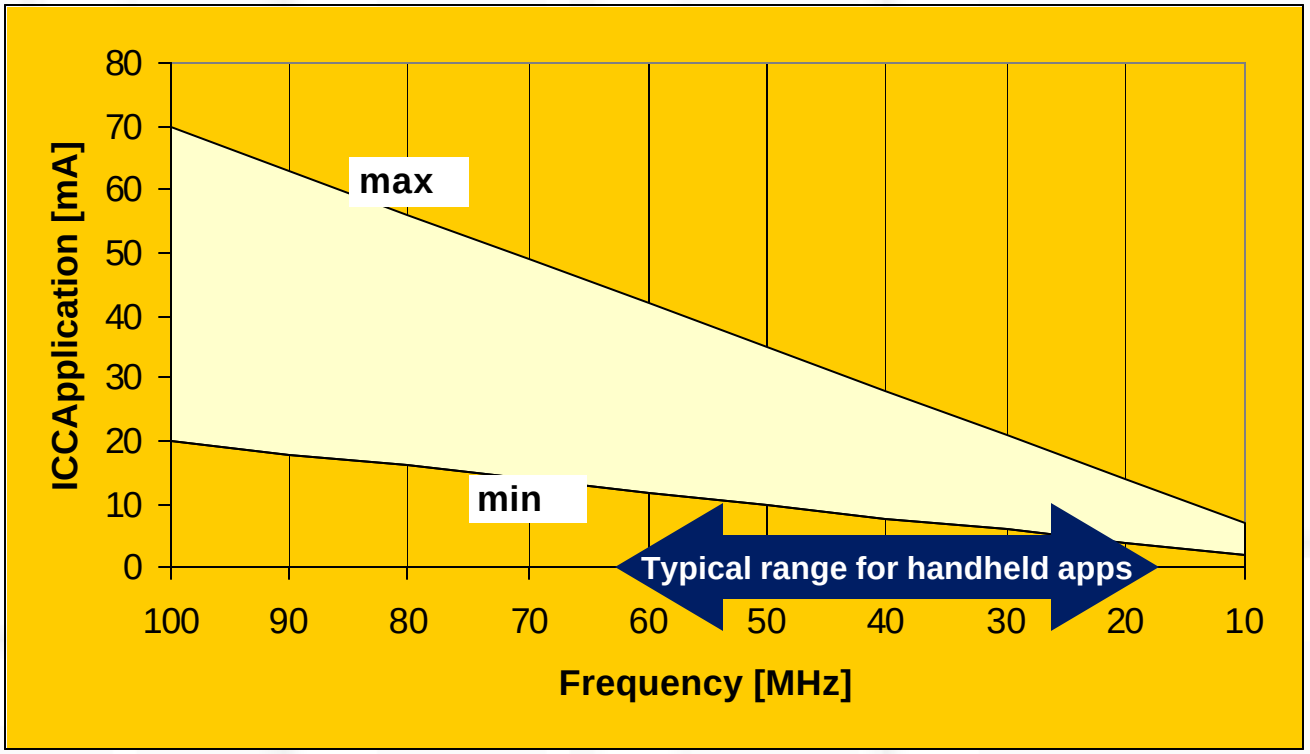
128M Mobile-RAM - Refresh Current

- Refresh current is strongly reduced to by partial array select and temperature-compensated self-refresh of Mobile-RAM



128M Mobile-RAM - Operating current

- The operating current is strongly dependent on frequency:



- Most handheld/mobile applications run memory at frequencies much lower than 100MHz
  - Operation at 20MHz reduces operating current to 4 - 14mA @VDD=2.5V

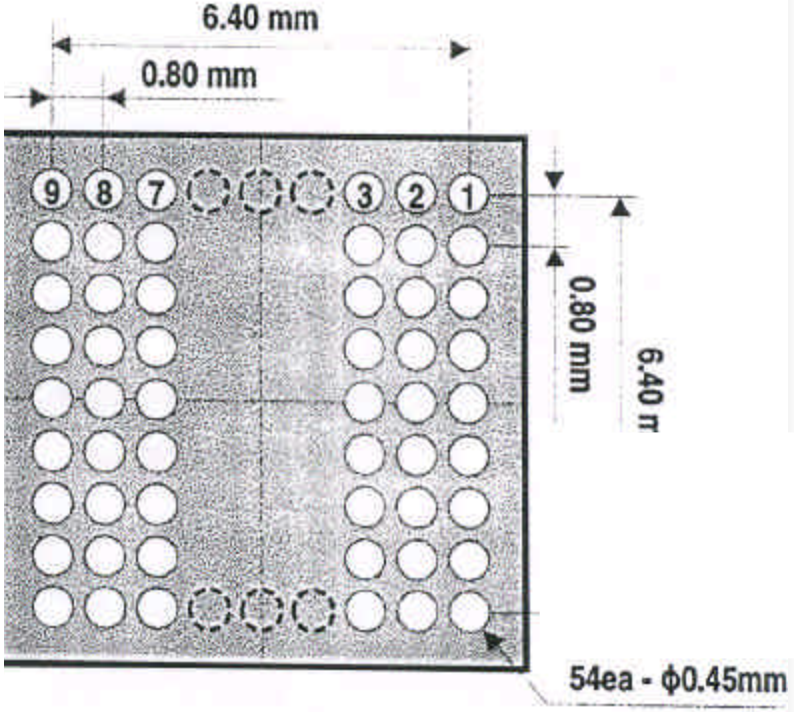
Mobile RAM Package
54-ball CSP/BGA

Pin-out:

1	2	3		7	8	9
VSS	DQ15	VSSQ	A	VDDQ	DQ0	VDD
DQ14	DQ13	VDDQ	B	VSSQ	DQ2	DQ1
DQ12	DQ11	VSSQ	C	VDDQ	DQ4	DQ3
DQ10	DQ9	VDDQ	D	VSSQ	DQ6	DQ5
DQ8	NC	VSS	E	VDD	LDQM	DQ7
UDQM	CLK	CKE	F	/CAS	/RAS	/WE
NC	A11	A9	G	BA0	BA1	/CS
A8	A7	A6	H	A0	A1	A10
VSS	A5	A4	J	A3	A2	VDD

< Top View >

Footprint:

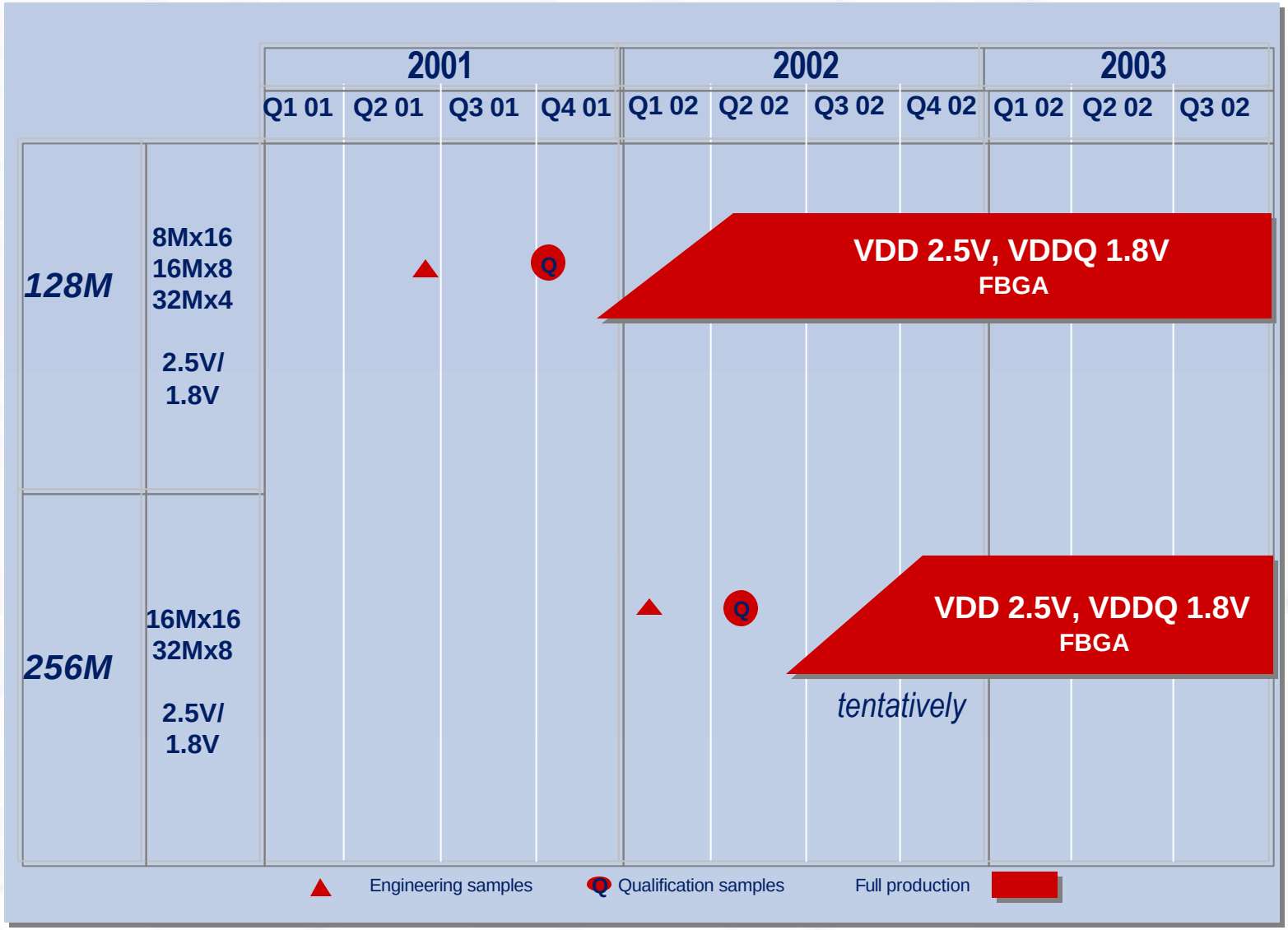


< Bottom View >

Mechanical outline: 8mm x 9mm

- FBGA package optimized for space-constrained applications

Mobile-RAM - Product Roadmap



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- **DDR Products using CSP**
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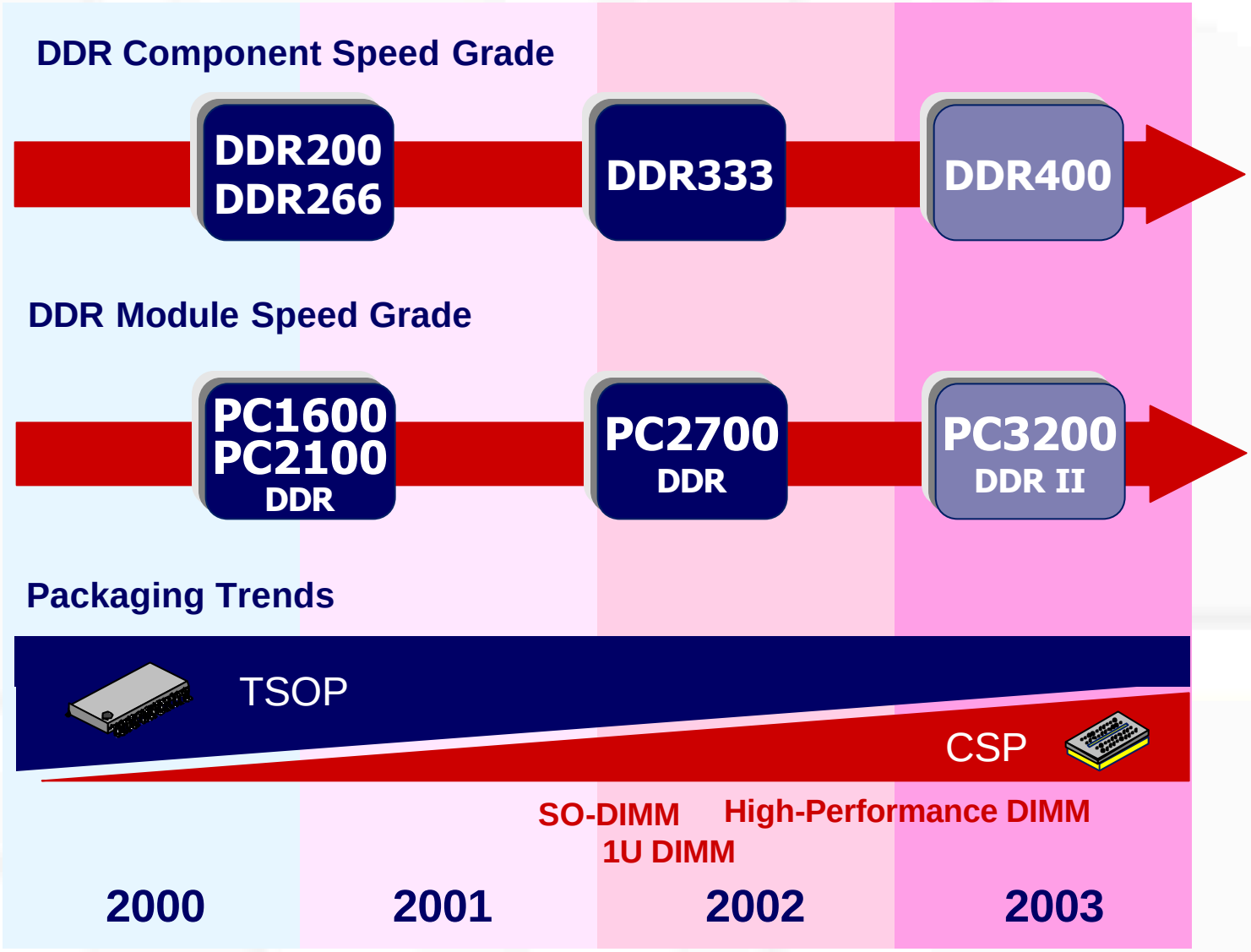
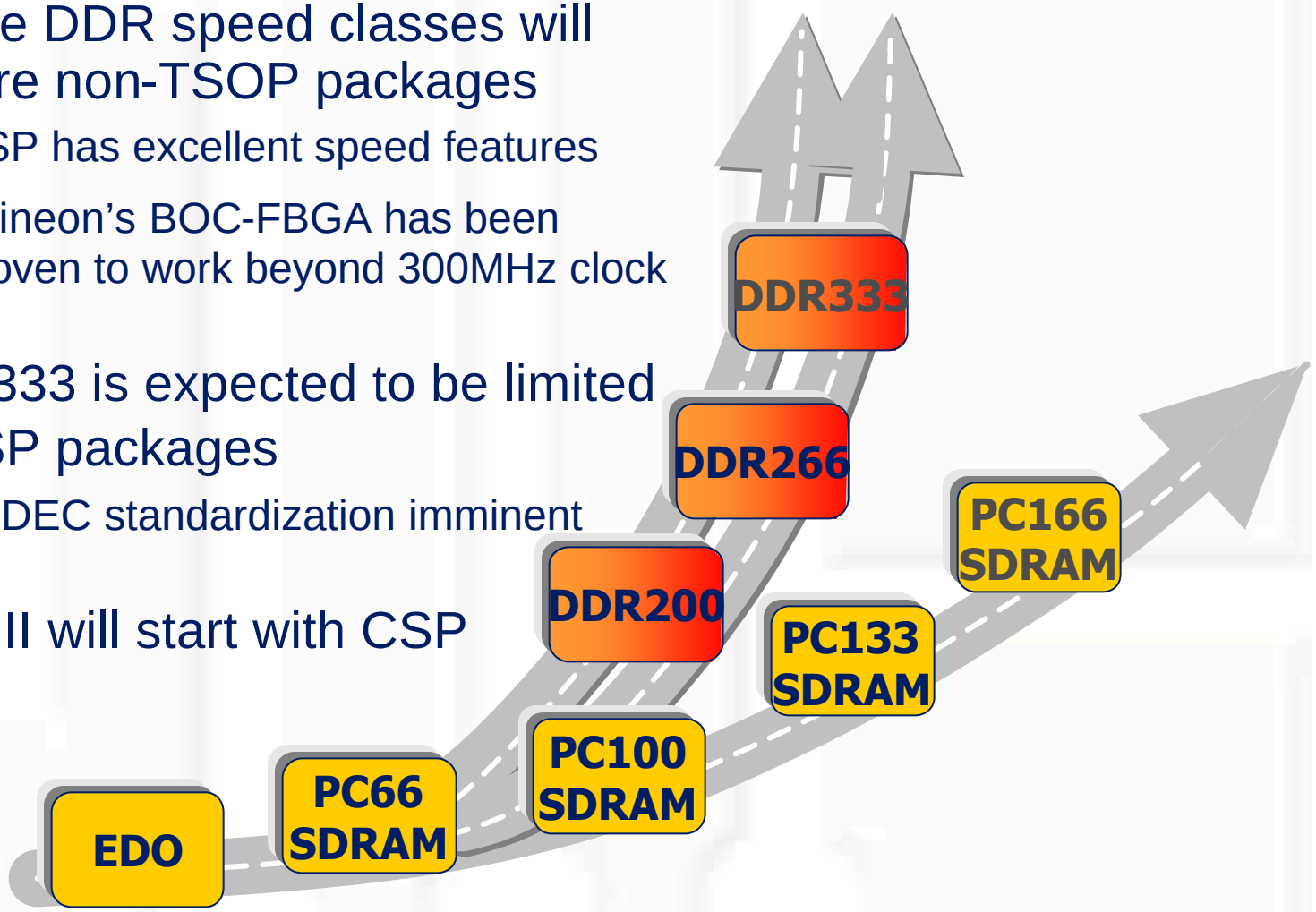
DDR Speed Roadmap

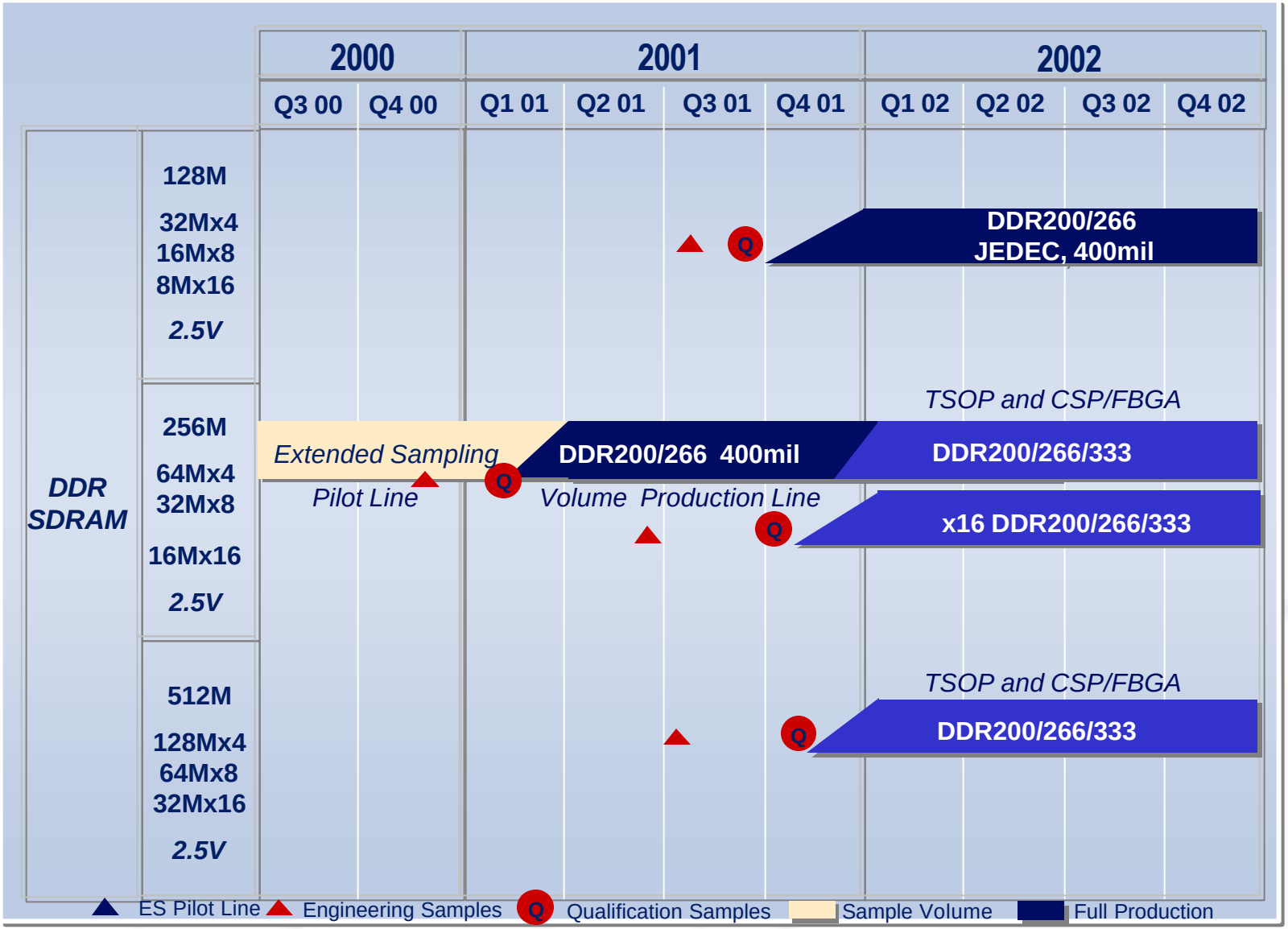


DDR Speed Roadmap

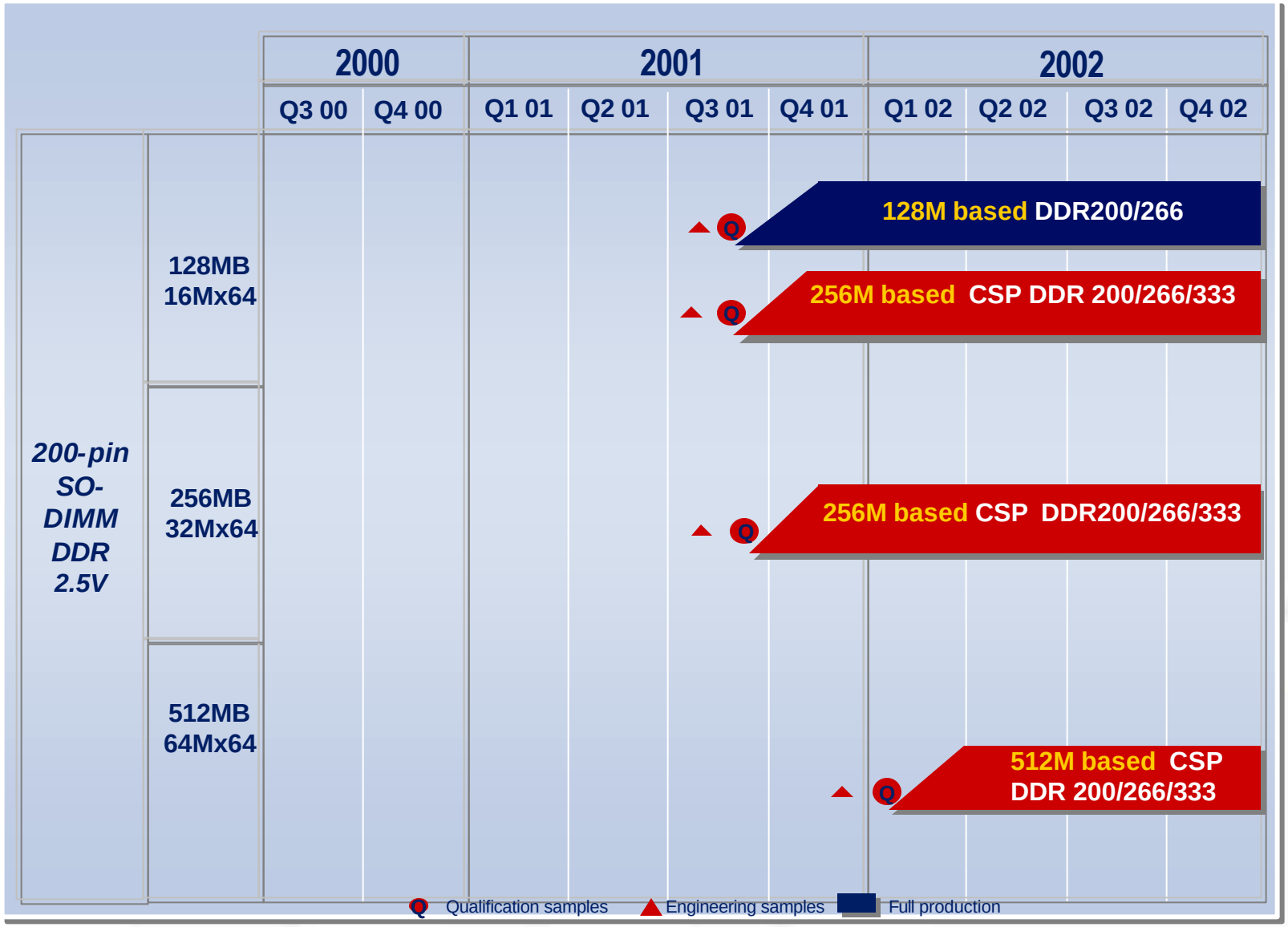
- Future DDR speed classes will require non-TSOP packages
  - CSP has excellent speed features
  - Infineon's BOC-FBGA has been proven to work beyond 300MHz clock
- DDR333 is expected to be limited to CSP packages
  - JEDEC standardization imminent
- DDR II will start with CSP



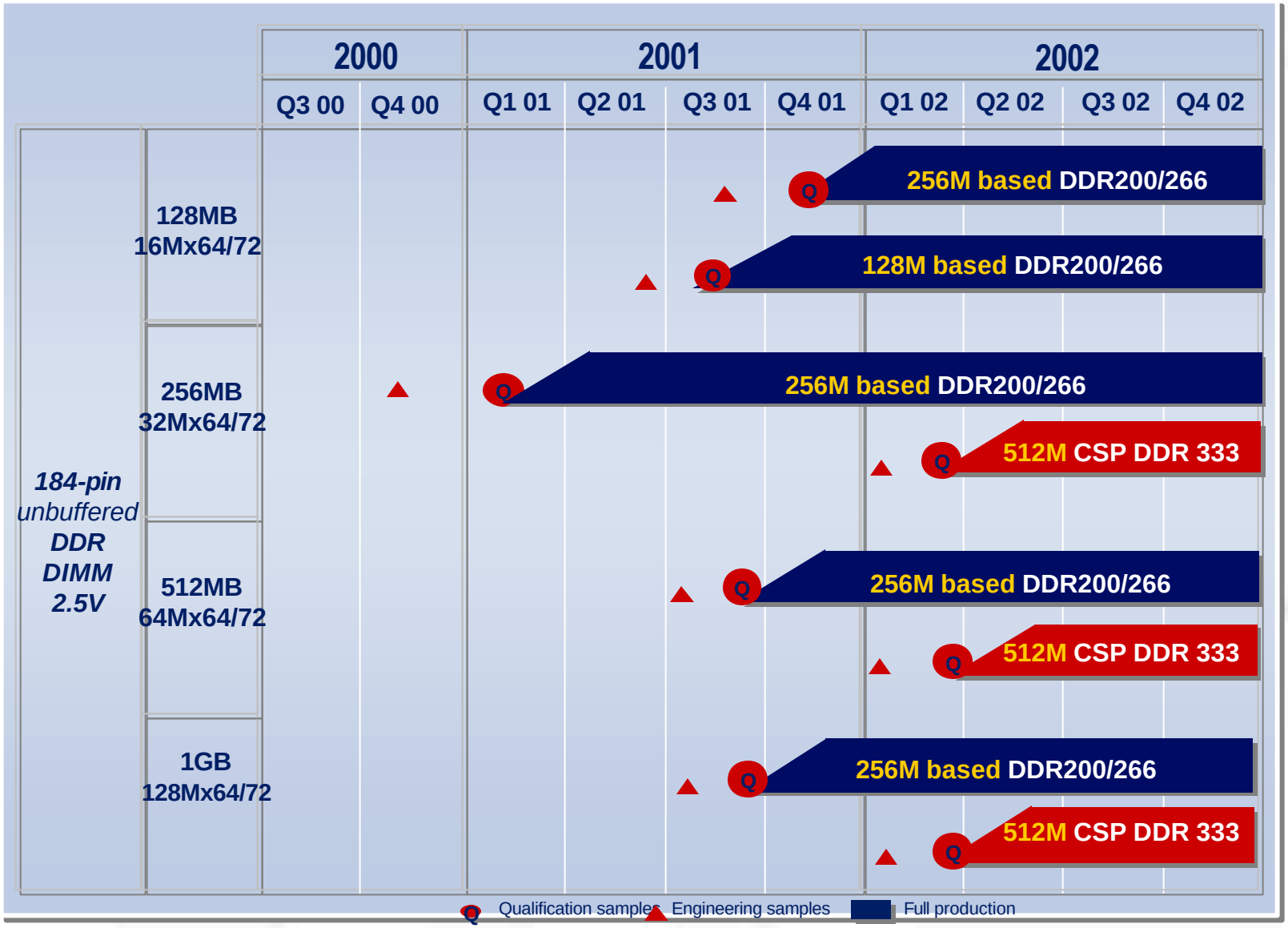
DDR: Product Roadmap



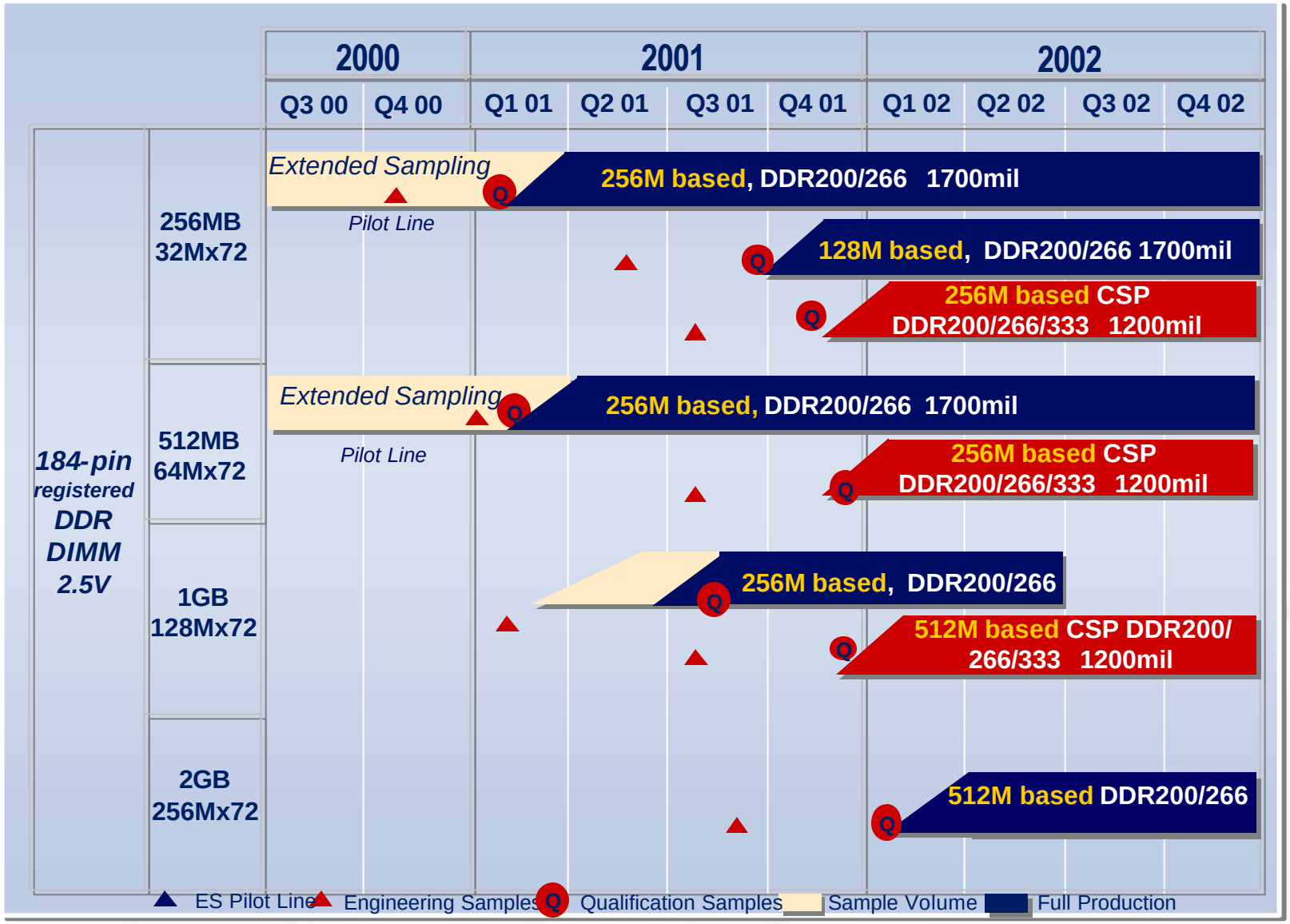
200-pin SO-DIMM DDR Modules



184-pin unbuffered DIMM DDR Modules



184-pin registered DIMM DDR Modules



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128M SGRAM Features

- Graphics-oriented DDR SDRAM organized 4M x 32
- Designed for up to 300MHz clock operation
  - Equivalent to 600Mbit/s/pin
- High-speed operation requires CSP package
  - P- LFBGA 128 was chosen
    - Inexpensive package targeted at consumer market
    - Excellent high-frequency properties
- Low-speed variant will be offered in TQFP

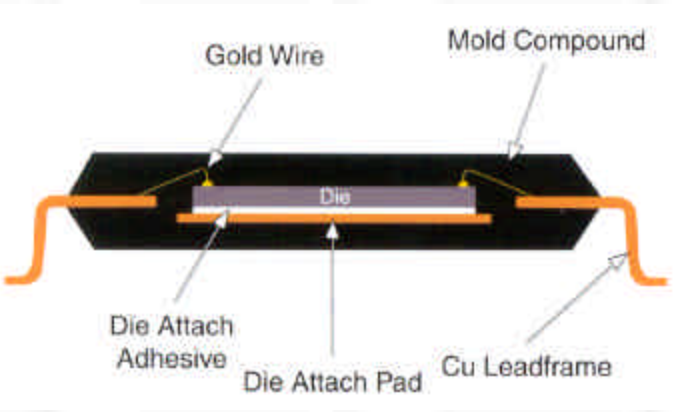
128M SGRAM in LFBGA

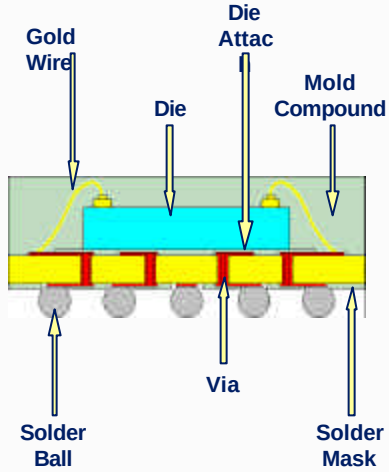
SGRAM Package

TQFP 100

LFBGA 128

Schematic cross sectior

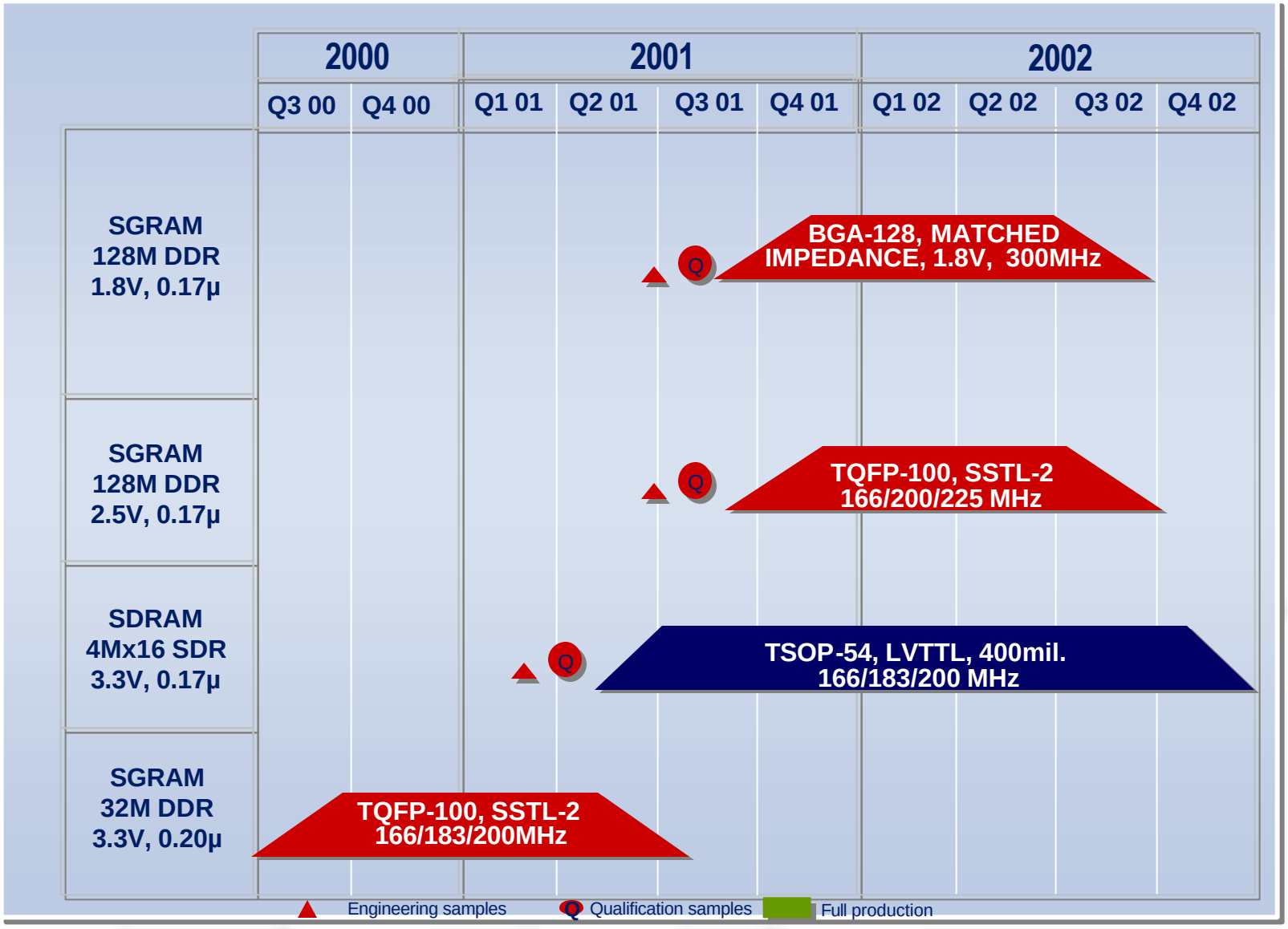




Features

Thermal Resistance	**R_{th}**	- 25 %
Electrical Performance	**Inductance**	- 30 %
Space Saving	**Board space**	- 57 %

Graphics Product Roadmap



CSP Memory Packages
Conclusion and Outlook

- Clock speed and silicon feature size will drive new packaging technologies
- Transition from inline packages (TSOP) to area array chip scale packages (FBGA-BOC)
- FBGA-BOC emerges as new standard package for high performance, high density memory
  - high electrical performance by shorter electrical paths
  - high thermal performance by shorter thermal paths
  - high density module by low space consumption
- Outlook:
  - Increased density will drive development into the 3rd dimension
  - Integrated assembly and test plus minimum footprint will drive Wafer-Level-Packaging